What is claimed is:

1. A method for use with a computer system, comprising:

permitting a first bus agent to access a bus during windows of time and preventing the first bus agent from accessing the bus outside of the windows to permit a second bus agent to access the bus, the first bus agent having a higher priority than the second bus agent;

monitoring use of the bus by the second bus agent during the windows; and

selectively regulating the durations of the windows based on the use.

2. The method of claim 1, wherein the first bus agent comprises:

a system controller.

3. The method of claim 1, wherein the second bus agent comprises:

a processor.

4. The method of claim 1, wherein the act of monitoring comprises:

determining a number of clock cycles in which first bus agent accesses the bus during the window.

5. The method of claim 1, wherein the act of regulating comprises:

decreasing the duration of one of the windows if the amount of use by the first bus agent approximately increases above a threshold.

6. The method of claim 1, wherein the act monitoring comprises:

counting clock cycles when the first bus agent requests ownership of the bus.

7. The method of claim 1, wherein the bus comprises:

a local bus.

8. The method of claim 1, wherein the bus comprises:
a Pentium Pro bus.

9. A method for use with a computer system, comprising:
permitting a first bus agent to access a bus during predetermined windows of time, the first bus agent having a lower priority than a second bus agent;
preventing the second bus agent from accessing the bus during the windows;
monitoring use of the bus by the first bus agent during the windows; and
selectively regulating the duration of the window based on the use.

10. The method of claim 9, wherein the first bus agent comprises:
a processor.

11. The method of claim 9, wherein the second bus agent comprises:
a system controller.

12. The method of claim 8, wherein the act of monitoring comprises:
determining a number of clock cycles in which the first bus agent accesses the bus during the window.

13. The method of claim 9, further comprising:
permitting the second bus agent to access the bus after the expiration of the window.

14. The method of claim 9, wherein the act of regulating comprises:
decreasing the duration of one of the windows if the amount of use by the first bus agent approximately decreases below a threshold.

15. The method of claim 9, wherein the act of monitoring comprises:

not counting clock cycles when the first bus agent accesses the bus.

16. A computer system comprising:

a local bus;

a processor coupled to the local bus;

a system controller coupled to the local bus, the system controller having a higher priority than the processor for bus arbitration; and

a circuit adapted to:

permit the system controller to access the bus during windows of time and prevent the system controller from accessing the bus outside of the windows to permit the processor to access the bus,

monitor use of the bus by the system controller during the windows, and

selectively regulate the durations of the windows based on the use.

17. The computer system of claim 16, wherein the circuit comprises:

a timer adapted to determine a number of clock cycles in which the system controller accesses the bus during one of the windows.

18. The computer system of claim 16, wherein the circuit is adapted to regulate the durations by decreasing the duration of one of the windows if the amount of use of the bus by the system controller approximately increases above a threshold.

19. The computer system of claim 16, wherein the circuit comprises:

a timer adapted to not count clock cycles when the processor accesses the bus and count clock cycles when the system controller accesses the bus.

20. A computer system comprising:

a local bus;

a processor coupled to the local bus;

a system controller coupled to the local bus and having a higher arbitration priority than the processor; and

a circuit adapted to:

permit the processor to access the bus during predetermined windows of time,

prevent the system controller from accessing the bus during the windows,

monitor use of the bus by the processor during the windows, and

selectively regulate the durations of the windows based on the use.

21. The computer system of claim 20, wherein the circuit comprises:

a timer adapted to determine a number of clock cycles in which the processor accesses the bus during one of the windows.

22. The computer system of claim 20, wherein the circuit is adapted to permit the system controller to access the bus after the expiration of one of the windows.

23. The computer system of claim 20, wherein the circuit is adapted to decrease the duration of one of the windows of the amount of use by the processor approximately decreases below a threshold.

24. The computer system of claim 20, wherein the circuit comprises:

a timer adapted to not count clock cycles when the processor accesses the bus and count clock cycles when the processor does not access the bus.